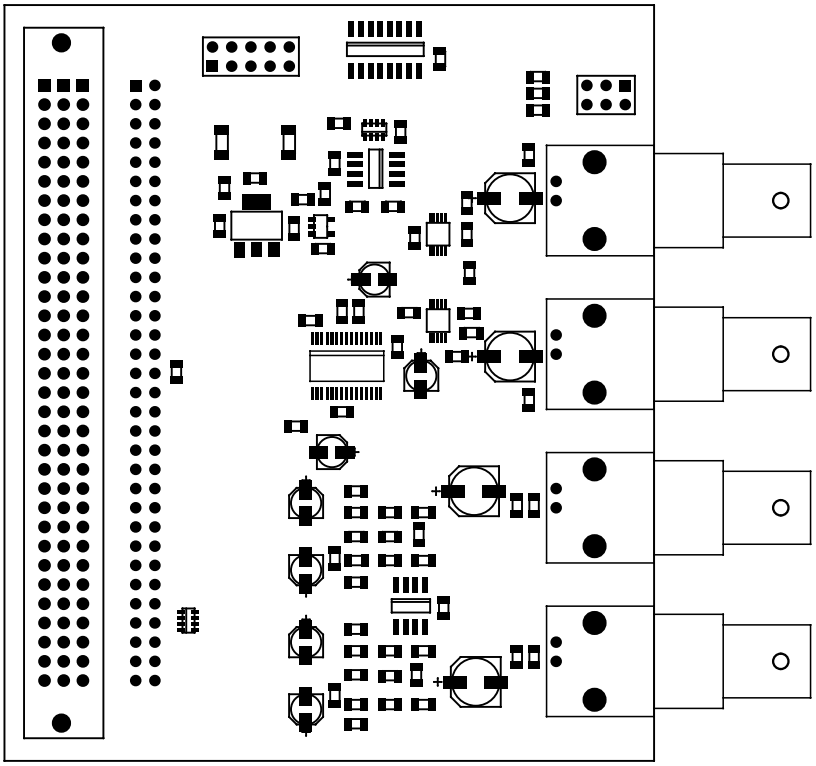
Danville Signal Processing, Inc.

dspstak™ c192k22



User Manual

Version 1.00

Danville Signal Processing, Inc.

dspstak™ c192k22 User Manual

Danville Signal Processing, Inc. strives to deliver the best product to our customers. As part of this goal, we are constantly trying to improve our products. Danville Signal Processing, Inc., therefore, reserves the right to make changes to product specification or documentation without prior notice. Updated operating manuals and product specification sheets are available at our website for downloading.

This manual may contain errors, omissions or "typo's". Please send your comments, suggestions and corrections to:

Danville Signal Processing, Inc.
29687 82nd Avenue Way
Cannon Falls, MN 55009

Trademark Notice

dspstak is a trademark of Danville Signal Processing, Inc. VisualDSP++, and SHARC are trademarks of Analog Devices, Inc. CyberClocks is a trademark of Cypress Semiconductor Corporation.

Contact Information

Danville Signal Processing, Inc.
29687 82nd Avenue Way
Cannon Falls, MN 55009

E-mail: dsp@danvillesignal.com
Web Site: http://www.danvillesignal.com

Voice: 507-263-5854
Fax: 877-230-5629

Table of Contents

Overview

DSP-based embedded applications often take the form of a digital signal processing engine coupled with a specialized data conversion and signal conditioning front end. The front end electronics and the DSP are almost always connected via high speed serial ports and the general purpose I/O ports of the DSP. In most cases, once the local memory and peripheral interfacing needs of the DSP are fulfilled, the DSP's data and address busses are no longer needed.

Standardized bus architectures such as PC/104, PCI and cPCI are all based on communicating via each board's data and address bus, while ignoring the needs of the most DSP / data conversion interfaces.

Introducing dspstak™

Danville's dspstak modules are designed to simplify DSP-based embedded applications. Generally, each dspstak consists of two modules: a DSP Engine, and a signal conditioning/data conversion I/O Module. The Interconnect Port consists of SPORTs (high speed serial ports), SPI, general I/O, clocks and power connections.

DSP Engine modules generally consist of a DSP processor, memory, power supplies and standard digital I/O such as RS-232 and USB. We currently have products based on Analog Devices' SHARC® processors.

The I/O Modules may include signal conditioning electronics, A/D and/or D/A data converters, audio transceivers, unique connectors and a plethora of other special front end requirements. Since the I/O Module is separate from the DSP Engine Module, custom interfaces can be created quickly and inexpensively. Danville has a number of standard I/O Modules and often is willing to create a new one based on customer request. You can also create your own.

dspstak™ c192k22

This manual covers the dspstak c192k22 I/O Module and is complemented by the dspstak Family Users Manual. The family manual covers topics that all dspstaks have in common. You will want to review the family manual for mechanical dimensions, system configurations, basic connector specifications, etc.

You will also need the relevant manuals and datasheets for the dspstak DSP Engine, the DSP processor and the data converter. Links to these manuals and other resources are found on our web site at http://www.danvillesignal.com/index.php?id=dspdev_links

Intended Audience

The dspstak c192k22 is intended for DSP systems integrators, designers and programmers who may wish to integrate a dspstak into their products. This manual is primarily aimed at users who have a working knowledge of microcomputer technology and DSP related design. We assume that you are familiar with the Analog Devices DSP used on the companion dspstak DSP Engine.

Introduction

The dspstak™ c192k22 is a two channel audio ADC & DAC I/O module based on an AKM AK4620A sigma delta codec. Assuming a 24.576 MHz master clock, the AK4620A allows a sampling rate of 192k with a resolution of 24bits. Other sampling rates are available by reprogramming the dspstak DSP Engine to another master clock frequency.

The dspstak c192k22 includes the following items:

Hardware:

- dspstak™c192k22 board

Documents & Programs (CD):

- This manual
- dspstak Family User Manual
- Device driver software

We recommend that you have the following tools and documents:

- Analog Devices VisualDSP++™ for SHARC®
- AKM AK4620A Data Sheet
- Documentation for the companion dspstak DSP Engine
- Cypress Semiconductor CyberClocks™

Our website (www.danvillesignal.com) has downloads and links to other supplementary tools and documents.

Hardware Description

The dspstak c192k22 I/O Module uses a sigma delta codec at its core. Sigma delta converters use noise shaping and oversampling to produce very good conversion results at much lower sample rates. One benefit of this technique is that antialiasing and anti-imaging filters are substantially less complex and critical since the actual sampling is performed at a much higher rate than the passband.

In the general case, you can change the sample rate by scaling the master clock. Sample rates as low as 8k are practical with this approach. Keep in mind that as the master clock frequency is reduced, the antialiasing and anti-imaging filters become less optimal since they do not scale with the sampling frequency. Of course, you can also perform sample rate conversion with the DSP processor to achieve other sample rates. This approach will yield the best performance at low sample rates.

Master clocks are provided by a dspstak DSP Engine. These clocks can be programmed to allow just about any arbitrary sampling rate from 8k to 204.8k. Examples:

- MCLK = 26.2144 MHz is used for 204.8k sampling (great for FFTs)
- MCLK = 24.576 MHz is used for 192k
- MCLK = 12.288 MHz is used for 96k, 48k, etc
- MCLK = 11.2896 MHz is used for 88.2k, 44.1k, etc.

Each audio input is buffered by a low noise programmable gain amplifier (PGA) stage. The PGA gain can be set independently for each input channel with gain settings of 1,2,4,5,8,10,16 or 32. In addition, the AK4620A has an internal PGA with a range 0f 0 to +18dB that can be adjusted in 0.5dB steps. The AK4620A has output attenuators that can be adjusted in 255 linear steps.

The following sections expand on the basic hardware of the dspstak c192k22:

- AKM AK4620A Codec
- MCLK Selection
- Input Buffer Amplifiers
- Output Buffer Amplifiers
- Power Supply
- Audio Connectors
- SPI Expansion
- LED Connections
- Optional Configurations
- Interconnect Port

AKM AK4620A Codec

The AK4620A is a high performance 24 bit codec with excellent dynamic range, S/N and filtering.

There are several different configurations that are possible with this device. In the dspstak c192k22, the codec is configured in PCM, Serial mode. The inputs are single ended to take advantage of the input PGAs available in the device.

The control port of the AK4620A is used to configure the sampling rates, PGAs, attenuators and other registers under software control. In the dspstak c192k22, these registers are all controlled by the dspstak SPI port using the #SS2 chip select. Software drivers are included with the dspstak c192k22 to illustrate the process. You will want to examine the source code in conjunction with the AK4620A datasheet to better understand and take advantage of all the various configuration options.

MCLK Selection

The dspstak c192k22 uses DAI4 as the source for its MCLK. This DAI pin is the output of a precision clock generator (PCG) on a third generation SHARC DSP (ADSP-2126x or ADSP-2136x). The input of the PCG is either MCLK0, MCLK1, DAI2 or the DSP's CLkIn. The PCG is a low jitter clock divider that allows the codec's MCLK to be divided by an integer (1 to N). This allows the codec to change sampling rates.

MCLK0 and MCLK1 are user reprogrammable clocks that are dedicated to I/O expansion. The frequency of these clocks can be set to many arbitrary frequencies. For example. They could be assigned to 24.576 MHz or 22.5792 MHz. This would allow the dspstak c192k22 to support both the 44.1/48k sets of preferred audio sample rates (up to 192k/176.2k).

You could also program MCLK0 or MCLK1 to 26.2144 MHz. This would support sample rates of 204.8k and lower. This might be desirable for systems implementing FFTs, since the frequency bins would be "nice" numbers.

The DAI2 pin is used for an external clock source. This could come from another dspstak I/O card such as an S/PDIF transceiver.

Input Buffer Amplifiers

A programmable gain amplifier (PGA) buffers each audio input. Signal levels should be restricted to +/- 2.8V full scale (2V rms sinusoid). The input impedance is 10K and is AC coupled. The high pass corner frequency is below 1Hz. The AK4620A has an internal HPF that also affects the low frequency response of the input. This filter can be bypassed via software control.

The PGA is set via SPI using the #SS3 chip select. Gains of 1,2,4,5,8,10, 16 and 32 are available with the external PGA. The AK4620A has an additional 0 to +18dB stepped PGA as well. This gain is controlled via the codec control registers.

Output Buffer Amplifiers

Third order anti-imaging filters are used to perform differential to single-ended conversion and remove high frequency noise from each DAC.

Power Supply

The dspstak c192k22 derives its operating power from its companion dspstak DSP Engine. The dspstak c192k22 operates entirely on a single positive supply. We recommend a 9VDC supply for the dspstak when operating in a c192k22 + DSP Engine configuration. Higher supply voltages may also be used with increased power dissipation since the analog 5 volt supply is derived using a linear regulator. There is no need for a negative or AC supply when using the dspstak c192k22 with a dspstak DSP Engine.

Audio Connectors

Standard BNC connectors are used for audio inputs and outputs. The board can also have optional connectors for special cases. These include SMA (only the left channel is supported) and MPC connectors. MPC connectors are a style used in PC computers, for example, the connection from a CD drive to a sound card. Consult Danville if you want to substitute the connector types.

SPI Expansion

The dspstak c192k22 has a 10 pin 0.100 header for digital I/O and SPI expansion. You might use this interface to create a control panel with push button switches, an LCD display or status LEDs.

Pin	Name	Notes
1	#RESET	
2	DGND	
3	Aux I/O	I/O
4	SPISO	MISO
5	Aux I/O	I/O
6	SPICLK	
7	SPISI	MOSI
8	#SPISS1	Slave Select or I/O
9	Vd+5	Not supported on all dspstak DSP Engines
10	Vd+3.3	

LED Connections

The dspstak c192k22 can be used for driving three optional LEDs. These are available via connections to JH1. JH1 is unpopulated but can be used as a convenient connection point for leaded LEDs. The LEDs are configured via SPI using the #SS5 chip select line.

Optional Configurations

A special version of the dspstak c192k22 is available as a subcomponent of the dspstak instrument. The dspstak c192k22 and a dspstak DSP Engine to combine as the internal electronics that fit into a housing that accommodates standard 3U (100 x 160mm) Eurocards. It this configuration the Interconnect Port DIN connector is installed on the opposite side of the pcb. The A & C rows of the connector are reversed. This is the reason, that the A & C rows of the DIN are connected together in the dspstak.

Interconnect Port

The Interconnect Port is the only standard connection between the DSP Engine and I/O Modules. This port is described in detail in the dspstak Family Users Manual and the DSP Engine manuals.

Row	A&C	B	Name	c192k22	Notes
1	*	*	AGND		Analog Ground
2	*	*	Va+		Unregulated Positive Analog Supply
3	*	*	Va-		Unregulated Negative Analog Supply
4	*	*	Va+5	Analog Supply	Regulated Analog +5.0 Volt Supply
5	*	*	AGND		Analog Ground
6	*	*	Vd+5		Digital 5.0 Volt Supply
7	*	*	Vd+3.3	Digital Supply	Digital 3.3 Volt Supply
8	*	*	DGND		Digital Ground – Main Return
9	*		SS1/IO0	Expansion SS	JH2 – 8
9		*	SS2/IO1	Codec SS	
10	*		SS3/IO2	PGA SS	
10		*	SS4/IO3		
11	*		SS5/IO4	LED SS	
11		*	DAI 2	Ext MCLK	
12	*		DAI 3	Aux I/O	JH2 - 3
12		*	DAI 1		
13	*		#SS0		
13		*	SPICLK	SCK	
14	*		SPISO	SO	
14		*	SPISI	SI	
15	*		DAI 4	MCLK	
15		*	#RESET		Codec & JH2 - 1
16	*		SYSCLKIN		
16		*	SYSCLK		
17	*		Vd+3.3		
17		*	GND		
18	*		DAI 5		
18		*	DAI 6		
19	*		GND		
19		*	MCLK0	I/O Clock	PCG input – connected to DAI15
20	*		DAI 7		
20		*	DAI 8		
21	*		DAI 9		

Row	A&C	B	Name	c192k22	Notes
21		*	DAI 10		
22	*		GP0		
22		*	GND		
23	*		DAI 11		
23		*	DAI 12		
24	*		GND		
24		*	Vd+3.3		
25	*		Vd+3.3		
25		*	GND		
26	*		DAI 13		
26		*	DAI 14	Aux I/O	JH2 - 5
27	*		GND		
27		*	MCLK1	I/O Clock	PCG input – connected to DAI16
28	*		DAI 15	PCG In	PCG input – connected to MCLK0
28		*	DAI 16	PCG In	PCG input – connected to MCLK1
29	*		DAI 17	LRCK	Codec I2S Interface
29		*	DAI 18	DT	Codec I2S Interface
30	*		GP1		
30		*	GND		
31	*		DAI 19	BICK	Codec I2S Interface
31		*	DAI 20	DR	Codec I2S Interface
32	*		GND		
32		*	Vd+3.3		

There are pads next to the Interconnect Port that connect to each pin of the connector. You may use these pins for custom interfaces or monitoring.

The I/O mapping of the c192k22 allows other I/O modules to be used at the same time provided that the I/O is mapped to non-conflicting pins. The dspstak™ S/PDIF I/O Module is compatible with the dspstak c192k22. This I/O module uses a male/female connector so that it can reside between the DSP Engine and the c192k22.

Register & Jumper Configuration

The AK4620A has separate control and data ports. The data port streams audio to and from the DSP using the DSP's SPORT interface. The control port uses an SPI interface to allow the DSP to read and write internal registers of the codec.

I2S Serial Interface

The dspstak c192k22 uses I2S interfacing for its audio data interface. I2S is an industry standard method invented by Philips to transfer a pair of samples between two audio devices. I2S supports a variety of word lengths; clocks can be supplied by either side of the interface or from an external clock source.

For the purposes of the dspstak c192k22, the interface transmits and receives 32 bit words for each channel. Unused bits are generally padded with zeros. The LRCK (left-right clock) and BICK (bit clock) are supplied by the AK4620A. These clocks are derived from MCLK (master clock), which is provided by the dspstak DSP Engine. The LRCK functions as the frame sync. It is a square wave operating at the sample rate frequency (Fs). BICK is 64xFs and is used as the shift clock.

Data is transmitted and received on the DT and DR lines, respectively.

You can learn more about the I2S interface by checking the relevant sections of the AK4620A and DSP manuals.

Codec Control Registers

The AK4620A codec is configured via SPI. It is used to set the sampling rate, configure the codec for the correct data interface, and adjust gain, attenuation and other operating parameters. These registers are described in the AK4620A datasheet and implemented in the dspstak c192k22 device drivers and example code.

Since SPI is a multi-device port, the dspstak c192k22 slave select line must be mapped to a unique SPI SS line. In the case of the dspstak c192k22, SS2# is used .

The AK4620A registers are described in detail in the AK4620A datasheet. The sample driver software will also help you configure the AK4620A for your needs.

Software

The Distribution CD includes software examples and device drivers that simplify the configuration of the dspstak c192k22. You may use these examples as take off points to start your own applications.

Our software library is constantly expanding. This code and other resources are available to our customers through our web site. Send an email to support@danvillesignal.com to gain access to the customer section of our web site.

Schematic

The Distribution CD includes a schematic diagram of the dspstak c192k22 in file sch_c192k22.pdf

Mechanical Drawings

Mechanical Drawings are included in the dspstak Family Users Manual. If you any need additional information on board mounting, clearances, etc, send an email to support@danvillesignal.com.

The dspstak can be incorporated into products in a variety of different ways. If you want to use the dspstak in an unusual configuration, you may want to check with us for suggestions, design review, etc.

Product Warranty

Danville Signal Processing, Inc. products carry the following warranty:

Danville Signal Processing products are warranted against defects in materials and workmanship. If Danville Signal Processing receives notice of such defects during the warranty period, Danville Signal Processing shall, at its option, either repair or replace hardware products, which prove to be defective.

Danville Signal Processing software and firmware products, which are designated by Danville Signal Processing for use with our hardware products, are warranted not to fail to execute their programming instructions due to defects in materials and workmanship. If Danville Signal Processing receives notice of such defects during the warranty period, Danville Signal Processing shall, at its option, either repair or replace software media or firmware, which do not execute their programming instructions due to such defects. Danville Signal Processing does not warrant that operation of the software, firmware, or hardware shall be uninterrupted or error free.

The warranty period for each product is one year from date of installation.

Limitation of Warranty:

The forgoing warranty shall not apply to defects resulting from:

- Improper or inadequate maintenance by the Buyer;
- Buyer-supplied software or interfacing;
- Unauthorized modification or misuse;
- Operation outside the environmental specification of the product;
- Improper site preparation and maintenance.

Exclusive Remedies:

The remedies provided herein are the Buyer's sole and exclusive remedies. In no event shall Danville Signal Processing, Inc. be liable for direct, indirect, special, incidental or consequential damages (including loss of profits) whether based on contract, tort, or any other legal theory.